FULL PAPER

Fully Printed Foldable Integrated Logic Gates with Tunable Performance Using Semiconducting Carbon Nanotubes

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The realization of large-area and low-cost flexible macroelectronics relies on both the advancements in materials science and the innovations in manufacturing techniques. In this study, extremely bendable and foldable carbon nanotube thin film transistors and integrated logic gates are fabricated on a piece of ultrathin polyimide substrate through an ink-jet-like printing process. The adoption of a hybrid gate dielectric layer consisting of barium titanate nanoparticles and poly(methyl methacrylate) has led to not only excellent gating effect but also superior mechanical compliance. The device characteristics show negligible amount of change after up to 1000 cycles of bending tests with curvature radii down to 1 mm, as well as very aggressive folding tests. Additionally, the electrical characteristics of each integrated logic gate can be tuned and optimized individually by using different numbers of carbon nanotube printing passes for different devices, manifesting the unique adaptability of ink-jet printing as a digital, additive, and maskless method. This report on fully printed and foldable integrated logic gates represents an inspiring advancement toward the practical applications of carbon nanotubes for high-performance and low-cost ubiquitous flexible electronics.

1. Introduction

Macroelectronics focuses on mechanical compliance and large area applications where the requirements on performance and integration density are less demanding.[1] Significant progress and demonstrations have already been made with examples ranging from electronic skins,[2] flexible and stretchable displays,[3] wearable electronics,[4,5] various stretchable sensors for human motion detection,[6,7] actuators,[8] and many more. The pioneering work in this area was initiated by the exploration of novel semiconducting materials including amorphous silicon, polysilicon, and organic semiconductors for thin-film transistors (TFTs) used in large area displays.[9,10] Although silicon and organic semiconductors have been the mainstream for many years, semiconducting inorganic nanomaterials, including carbon nanotubes,[11] nanosheets,[12] and nanowires,[13] have attracted significant amount of research interests during the past decade owing to their superior electrical performance, reliability, and low-cost processing. In particular, thin films of carbon nanotubes offer superior carrier mobility,[14] optical transparency, and mechanical flexibility,[15] and have been widely explored as both conductors[6,16] and channel materials[17,18] in compliant electronics. Furthermore, recent availability of the sorted high-purity semiconducting single-wall carbon nanotubes[19] (sSWCNTs) has enabled large-area and solution-based fabrication of flexible TFTs and integrated circuits with performance and air stability greatly exceeding their organic semiconductor counterparts.[20,21]

Practical applications of flexible electronics also rely on the innovations in manufacturing and packaging processes, the cost of which, instead of that of materials, usually dominates the cost of the end products.[10] Conventional processes adapted from the semiconductor industry usually involve photolithographic patterning and vacuum-based deposition and etching processes, which are usually associated with high cost. Alternatively, printing techniques, widely used in graphic arts and newspaper industries, could in principle enable low-cost and large-scale fabrication of macroelectronics.[22,23] Among the numerous printing methods available, gravure and screen printing are particularly suitable for large area fabrication while digital ink-jet printing is maskless and more flexible in terms of changing the layout design.[22] sSWCNT TFTs and integrated circuits have already been demonstrated using various printing methods.[24–27] However, most of the reports on sSWCNT-based integrated circuits involve either electrodes/interconnection patterned using photolithography[25] or dielectrics deposited using atomic layer deposition or other similar vacuum-based processes.[27] Here in this paper, we report fully printed carbon nanotube TFTs and integrated logic gates fabricated on an ultrathin flexible substrate. Our reported process results in devices with excellent performance, yield, uniformity, and robustness under aggressive folding tests. More importantly, we also demonstrate that the electrical characteristics of the logic gates can be tuned and optimized individually after they are fabricated, manifesting the unique flexibility and adaptability of the ink-jet printing method.[22,26]

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Additionally, dielectric layer with high permittivity is needed to enable low gate voltage operation. The realization of flexible and stretchable TFTs requires the dielectric material to be highly compliant, posing a greater challenge in the selection of suitable materials. Conventional ceramic dielectrics, such as SiO_2, Al_2O_3, and HfO_2, are fragile and usually require tricky recipes.[4,18,20] Alternatively, hybrid dielectrics consisting of polymers and nanoparticles are excellent platforms for mechanically compliant TFTs because they not only possess high dielectric constant and mechanical flexibility/stretchability but could also enable low-cost and scalable solution-based processing.[28] In this study, the printed TFTs adopt a hybrid dielectric ink comprised of barium titanate ($BaTiO_3$) nanoparticles and poly(methyl methacrylate) (PMMA), which offers excellent gating effect and low leakage current. The addition of PMMA also renders the TFTs and logic gates extremely flexible and even foldable. We have demonstrated that our devices could survive repeated bending tests (curvature radius < 1 mm) and very aggressive folding tests without showing noticeable change in the electrical characteristics.

2. Results and Discussion

2.1. Device Fabrication

Figure 1a illustrates the main steps involved in fabricating the fully printed flexible sSWCNT TFTs and integrated logic gates. Ultrathin substrates are essential to realize highly flexible electronics as the strain induced in the devices due to bending scales as $t/2R$, where t and R represent the substrate thickness and curvature radius, respectively.[4,29] Here, we used an ultrathin polyimide substrate with a thickness of around 10 μm that was spun coated on a silicon handling wafer. sSWCNT network with a density greater than 50 tubes μm^{-2} (Figure 1d) was deposited onto the substrate using the solution-based process described in our previous publications.[11,20] Then, silver (Ag) nanoparticle inks were printed to define the patterns of the source/drain (S/D) electrodes for the TFTs and interconnects for the logic gates. Next, $BaTiO_3$/PMMA inks were printed into the channel regions of the TFTs as the hybrid dielectric which also served as the hard mask for the subsequent etching of the sSWCNTs out of the channel regions. After etching the unwanted sSWCNTs, another layer of $BaTiO_3$/PMMA was printed into the channel regions to repair the damage caused by O_2 plasma and to avoid potential gate leakage. Ag top-gate electrodes were subsequently printed and annealed to complete the fabrication of TFTs. Finally, multiple passes of sSWCNTs were printed into channel regions of the load resistors, one layer at a time, until the optimal device characteristics were achieved. Once the fabrication was completed, the polyimide substrate was delaminated from the silicon handling wafer, resulting in the extremely flexible integrated logic gates as shown in Figure 1b. The optical image of a resistive load p-type-only inverter is presented in Figure 1c. Typical channel length (L) and channel width (W) of such printed TFTs are in the range of 50–150 μm and 520–580 μm, respectively.

2.2. Transistor Performance

Representative electrical characteristics of the fully printed sSWCNT TFTs are presented in **Figure 2**. Carbon nanotube transistors normally exhibit p-type behavior in ambient environment due to the oxygen and moisture adsorption.[30] The transfer characteristics (I_{SD}–V_{GS}) in Figure 2a exhibit a slight

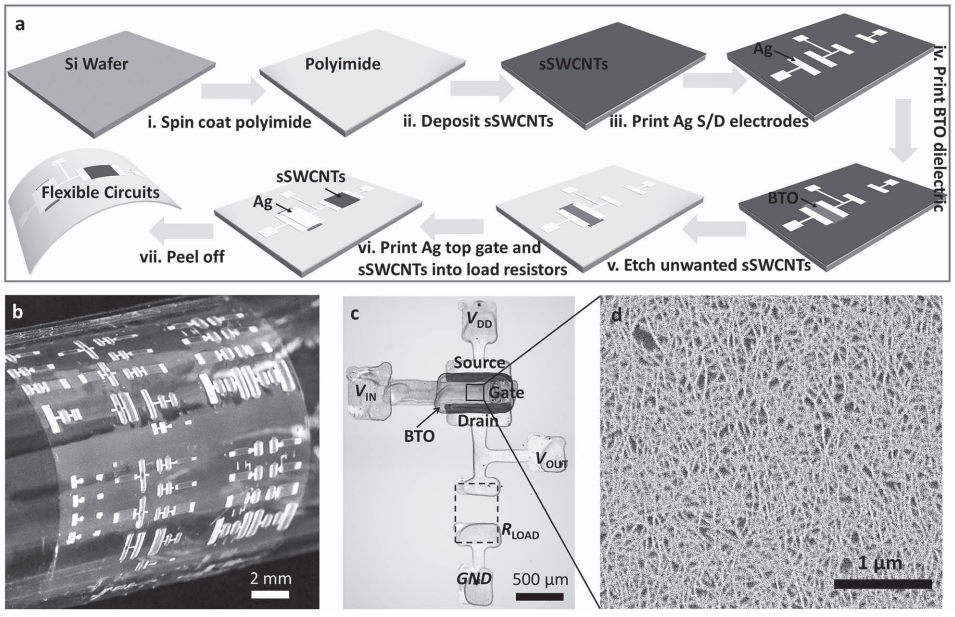

Figure 1. Fully printed and foldable carbon nanotube integrated circuits on ultrathin polyimide substrates. a) Schematic diagrams showing the fabrication process flow of a resistive load p-type-only inverter. b) Photograph showing printed nanotube circuits wrapped around a cylinder with a diameter of 27 mm. c) Optical image of a resistive load p-type-only inverter after all the layers are printed. d) Scanning electron microscope (SEM) image of the sSWCNT network in the channel region of the switching TFT.

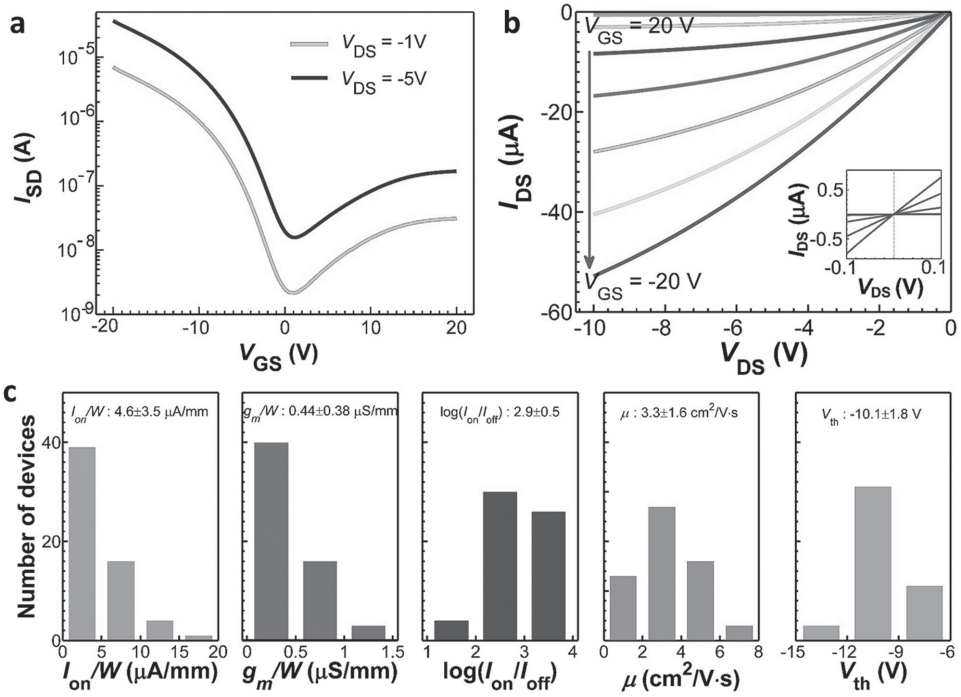

Figure 2. Electrical characteristics of the fully printed top-gated nanotube TFTs. a) Transfer characteristics of a representative device (L = 90 μm, W = 560 μm) measured with V_{DS} of –1 and –5 V. b) Output characteristics of the same device with V_{GS} varying from 20 to –20 V. Inset: Output curves at low source–drain voltages (triode region) implying ohmic contacts between the nanotubes and Ag electrodes. c) Histograms showing the statistical distributions of TFT performance metrics obtained from over 70 devices. From left to right: channel width–normalized on-current and transconductance, on/off current ratio, field-effect mobility, and threshold voltage.

ambipolar behavior with a predominant p-type branch, which is expected as the TFTs are top-gated devices with carbon nanotubes fully passivated by the gate dielectric layer. Figure 2b presents the output characteristics (I_{DS}–V_{DS}) of the same device with V_{GS} ranging from 20 to –20 V, exhibiting unambiguous current saturation that is typical for conventional field-effect transistors. The highly linear I_{DS}–V_{DS} curves measured under small V_{DS} (inset of Figure 2b) further indicate the low electronic barriers between the silver S/D electrodes and the sSWCNT network. In addition, unlike back-gated carbon nanotube TFTs that exhibit large hysteresis, the hysteresis in top-gated TFTs is greatly suppressed, due to the encapsulating by the $BaTiO_3$/PMMA layer (Figure S1, Supporting Information).

Gate capacitance is a critical parameter in determining the field-effect mobility (μ) of field-effect transistors. In most literatures, the gate capacitance of sSWCNT TFTs is calculated using either an ideal parallel-plate model or a more rigorous cylindrical model. However, the former typically overestimates the gate capacitance due to the porous nature of the nanotube network and thus underestimates the device mobility, while the latter may overestimate the mobility due to the uncertainty in determining the nanotube diameter and density of a random network. Here, we conducted capacitance–voltage measurements (see Figure S2, Supporting Information) on the TFTs to precisely determine their gate capacitance, which was in turn used to accurately assess the field-effect mobility. The highest and average values of the mobility were found to be 9 and 3.3 $cm^2\ V^{-1}\ s^{-1}$, respectively. The high-density sSWCNT network in the channel region also results in large width-normalized on-current (I_{on}/W) with a maximum value of 15 μA mm^{-1} and an average value of 4.6 μA mm^{-1}, measured at a V_{DS} of –1 V. The on/off current ratio (I_{on}/I_{off}) remains to be above 10^3 on average, sufficient for most logic gate applications. The I_{on}/I_{off} reported here is respectable for the 98% sSWCNT ink used and can be further improved by using inks with a higher purity of semiconducting nanotubes. Detailed statistical distributions of the device performance metrics, including I_{on}/W, width-normalized transconductance (g_m/W), I_{on}/I_{off}, μ, and threshold voltage (V_{th}), of over 70 TFTs are shown in Figure 2c, exhibiting good device-to-device uniformity for a fully printed fabrication process.

It is worth noting that a solution-based drop-coating process was used to deposit the sSWCNT network as the semiconducting channel material throughout the substrate. Although, strictly speaking, the sSWCNTs were not printed, the drop-coating method is still in principle compatible with the roll-to-roll printing process. As a comparison, we have also fabricated fully printed back-gated TFTs on rigid silicon substrates, where the sSWCNTs were deposited only into the channel region via the same printing method as that used for the Ag electrodes. This is a more cost-effective approach in terms of sSWCNTs usage compared with drop-coating method. However, as shown in Figure S3 (Supporting Information), such devices exhibit inferior uniformity compared with the devices shown in Figure 2, which can be attributed to the difference in the uniformity of nanotube networks obtained from the printing and drop-coating methods. Therefore, it is essential to further optimize the printing process for depositing sSWCNTs in the

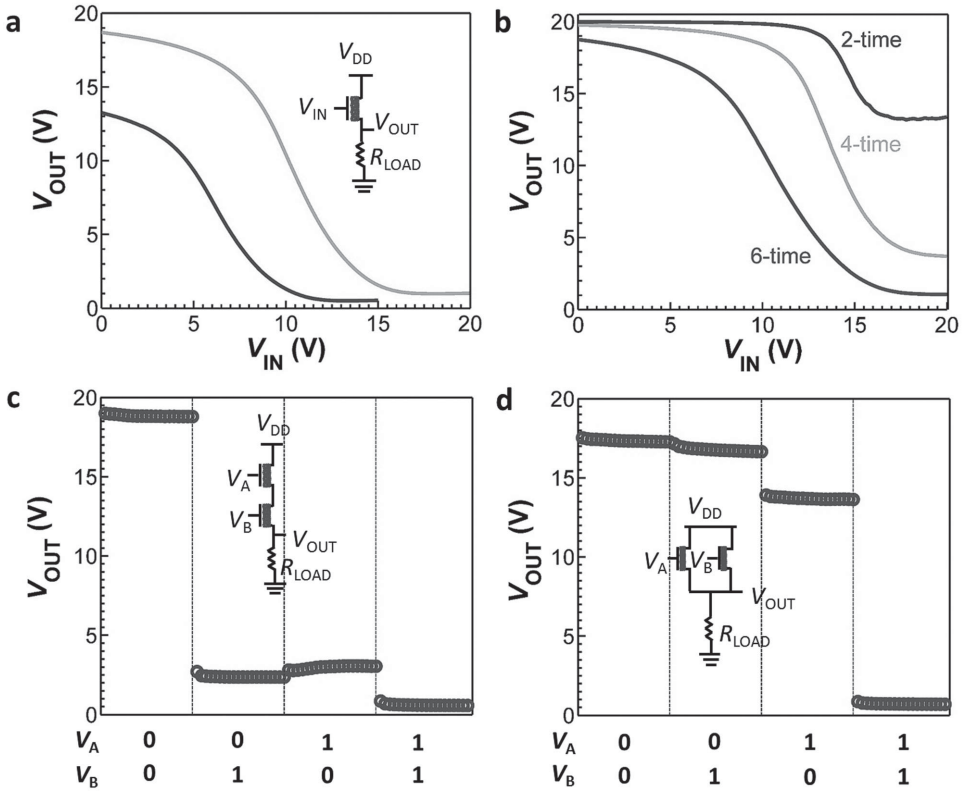

Figure 3. Electrical characteristics of the fully printed logic circuits. a) Voltage transfer characteristics (VTCs) of a resistive load p-type-only inverter measured with V_{DD} of 15 and 20 V. Inset shows the circuit diagram of the inverter. b) VTCs of the inverter with two-time, four-time, and six-time printing of sSWCNTs into the load resistor, showing the feasibility of tuning the inverter performance after the circuit has been fabricated. Output characteristics of the resistive load 2-input c) NOR and d) NAND d) gates. The supply voltage V_{DD} is 20 V for both circuits. Input voltages of 20 and 0 V are treated as logic "1" and "0," respectively. The corresponding circuit diagrams are shown as insets.

future in order to achieve both high cost effectiveness and uniform device performance.

2.3. Logic Gate Performance

Figure 3 presents the electrical characteristics of the fully printed logic gates, including resistive load p-type-only inverters (Figure 3a,b), 2-input NOR (Figure 3c), and 2-input NAND (Figure 3d) gates. The inset of each panel illustrates the corresponding circuit diagram. The inverter voltage gain extracted from the voltage transfer characteristics (VTC) in Figure 3a ranges from 2 to 4, which is acceptable for a fully printed device with a resistive load and is comparable with the results in literature. For the NAND and NOR gates, both exhibit excellent output characteristics with unambiguous logic "0" and "1" states, which coincide very well with the anticipated output values for each combination of the input states.

One unique advantage of the ink-jet based printing process is its flexibility, allowing the performance of each device to be tuned individually. As an example, when fabricating the logic gates, we printed multiple passes of sSWCNTs into the load resistor to fine adjust its conductance and thereby pull-down strength, until the optimal inverter VTC was achieved. As shown in Figure 3b, the inverter VTC underwent stepwise improvement (reduced logic "0" voltage) after the sSWCNTs were printed into the load resistor for two, four, and six times. In theory, the output voltage at any given input voltage can be determined from the voltage division between the channel resistance of the switching TFT and the load resistance as illustrated in Figure S4 (Supporting Information). Therefore, in order to achieve the optimal inverter VTC, the load resistance (R_{LOAD}) needs to fall between the on-state and off-state channel resistance of the switching TFT (R_{TFT}). If the R_{LOAD} is too large (small), it would make the inverter difficult to be pulled down (up), resulting in an increased logic "0" voltage (decreased logic "1" voltage). Printing more sSWCNTs into the load resistor could result in a higher network density (Figure S4a, Supporting Information), which in turn decreases the R_{LOAD} drastically (Figure S4c, Supporting Information). The simulated inverter VTCs after different times of sSWCNT printing (Figure S4e, Supporting Information) derived using the equation given in Figure S4b (Supporting Information) agree well with the measured VTCs presented in Figure 3b. The results presented here imply that the performance of each element can be tuned individually during or post the fabrication process, reflecting the unique flexibility of the ink-jet printing method, which cannot be achieved by other fabrication methods such as gravure printing or conventional lithography-based approaches.

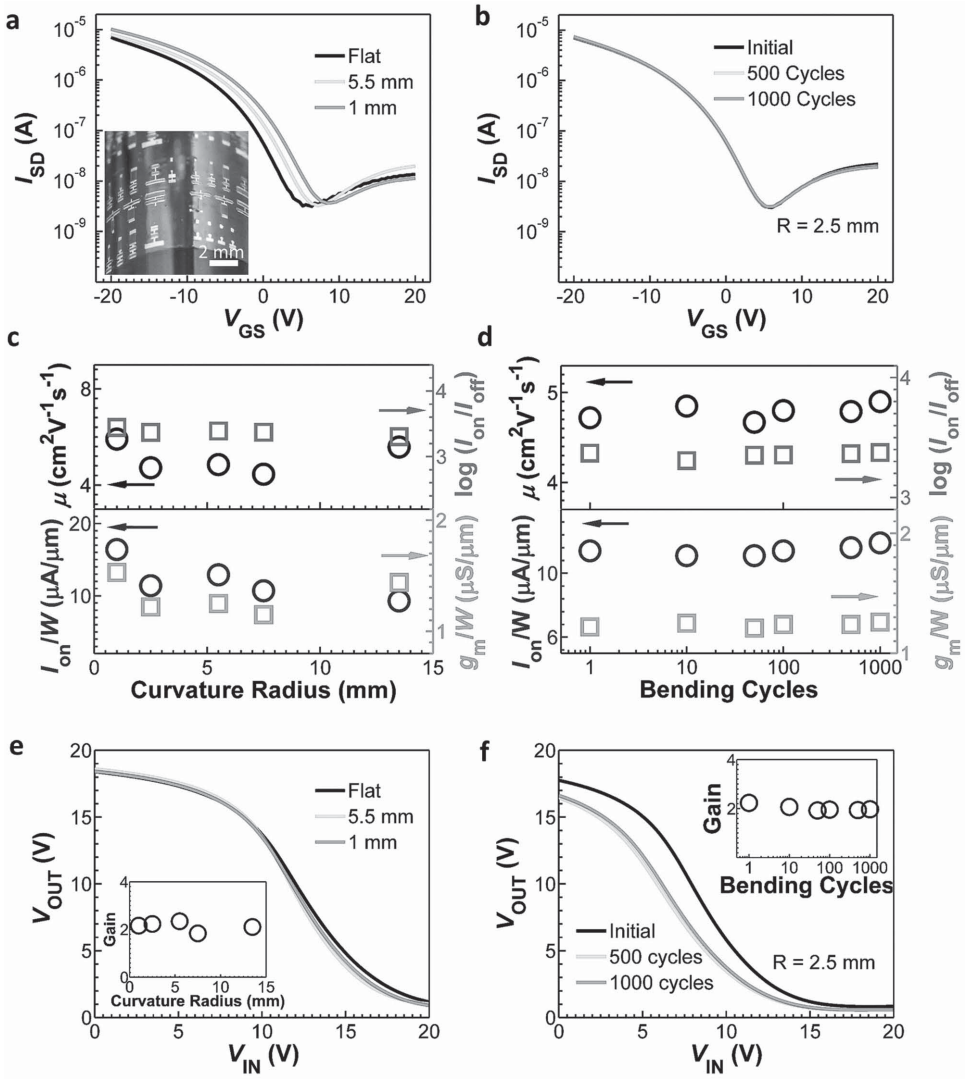

Figure 4. Bending tests on the fully printed nanotube TFTs and circuits. Transfer characteristics of a nanotube TFT measured a) at various curvature radii and b) after various numbers of bending cycles with a curvature radius of 2.5 mm. Insets of (a): Photograph of the circuits being wrapped around a cylinder with a curvature radius of 13 mm. TFT performance metrics, including channel width–normalized on-current and transconductance, field-effect mobility, and on/off current ratio as functions of c) curvature radius and d) bending cycles. All metrics exhibit negligible variations down to a curvature radius of 1 mm and after 1000 cycles. Inverter VTCs measured e) at various curvature radii and f) after various numbers of bending cycles. Insets in panels (e) and (f) show the inverter gain as functions of curvature radius and bending cycles, respectively, indicating the excellent flexibility and reliability of the circuit.

2.4. Bending and Folding Test

Figure 4 shows the results of systematic bending tests conducted on the fully printed TFTs and logic gates. The transfer characteristics of the TFTs exhibit only minimal variations when bent down to curvature radii of as small as 1 mm (Figure 4a), and remain essentially unchanged throughout the process of up to 1000 bending cycles (Figure 4b) with a curvature radius of 2.5 mm. The extracted TFT performance metrics, including channel width–normalized on-current and transconductance, on/off current ratio, and field-effect mobility are plotted as functions of curvature radius and bending cycles in Figure 4c,d, respectively. All TFT metrics exhibit excellent stability during the entire bending tests. In addition, the inverter VTC and gain also exhibit negligible variations while the device is bent to various curvature radii down to 1 mm and for up to 1000 cycles (Figure 4e,f). The excellent flexibility and reliability of our fully printed TFTs and logic gates can be attributed to the small thickness of the polyimide substrate used. For a substrate thickness of 10 μm as used in this study, the tensile strain on the outer surface is only 0.5% for a curvature radius of 1 mm, which is well below the elastic limit of all components (Ag electrodes, $BaTiO_3$ dielectric, and sSWCNTs network) of the devices.

Impressively, our fully printed devices are so robust that they can even be folded to extreme conditions that are well beyond the need for typical applications. The TFTs and logic gates could survive very aggressive deformation such as squeezing using a tweezer as shown in Figure S5a (Supporting

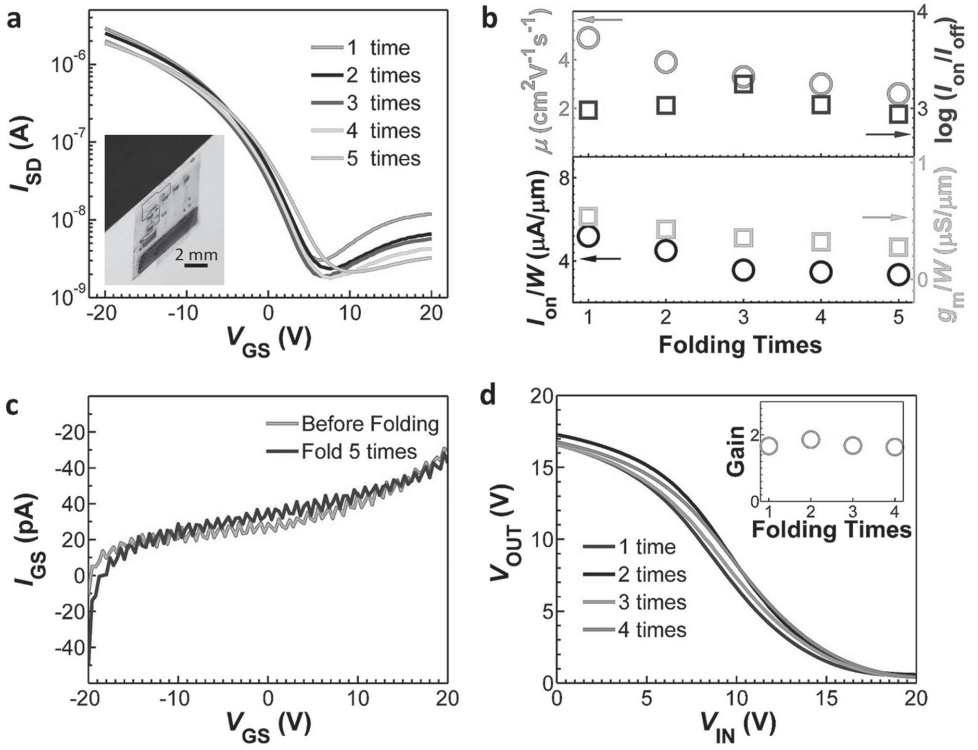

Figure 5. Folding tests on the fully printed nanotube TFTs and circuits. a) TFT transfer characteristics measured after multiple times of folding. Inset: Photograph of the circuit being folded over the edge of a piece of paper. b) TFT performance metrics, including channel width–normalized on-current and transconductance, field-effect mobility, and on/off current ratio after multiple times of folding. c) Gate–source current before and after folding for five times, showing the gate leakage current remains unchanged after the folding test. d) Inverter VTCs measured after several times of folding. Inset: Inverter gain as a function of folding times. The electrical characteristics of both the TFT and the inverter exhibit excellent reliability during the aggressive folding test.

Information). **Figure 5**a shows that the transfer characteristics of a TFT exhibit only minor variations after five times of aggressive folding tests. The inset photograph gives an example of the device being folded over the edge of a piece of paper. The TFT performance metrics are extracted and presented in Figure 5b as functions of folding times, manifesting the excellent reliability of our devices. Furthermore, as shown in Figure 5c, the gate leakage current was essentially unchanged and remained below 40 pA after five times of folding and squeezing by a tweezer, demonstrating the superior robustness of the $BaTiO_3$/PMMA hybrid dielectric layer. Similarly, the inverter VTC also remained nearly unchanged during the folding tests as shown in Figure 5d.

The superior robustness of the gate dielectric layer could be attributed to the addition of PMMA that acts as binders between $BaTiO_3$ nanoparticles. The $BaTiO_3$/PMMA composite could be more suitable than conventional ceramic dielectric materials for flexible electronics because they are not only more mechanically compliant but also printable, which is especially beneficial for the low-cost and large-scale fabrication. The tensile strain exerted onto the dielectric layer is estimated to be ≈20% when the sample is folded over the edge of a piece of paper (inset of Figure 5a) and could be well beyond that value when squeezed by a tweezer (Figure S5, Supporting Information). This implies that our devices could potentially be stretchable provided that suitable substrate and conductive materials were used. The results indicate the composite dielectrics consisting of inorganic nanomaterials and polymers are perfect choices for flexible/stretchable electronic devices since they combine the best of both worlds to provide functionalities and advantages that are lacked in either component alone.[28]

For our previously reported flexible integrated circuits fabricated using conventional microfabrication processes,[20] the bottleneck is mainly the fragile ceramic Al_2O_3 gate dielectric that cracks way before the metal thin film and sSWCNT network upon aggressive bending/folding. In contrast, for the fully printed circuits reported in this work, despite the fact that they are already much more flexible than before, the bottleneck was found to be the printed Ag interconnects rather than the dielectric layer. As can be seen from the optical image in Figure S5b (Supporting Information), although the gate dielectric remains almost intact, the printed Ag features start to crack and delaminate from the substrate after repeated folding to extreme conditions, indicating the fragileness of the Ag features and the relatively weak adhesion between the printed Ag nanoparticles and the polymer substrate. The irreversible damage in the Ag electrodes leads to a gradual increase in the electrode resistance, which is responsible for the decrease in the on-current and mobility as shown in Figure 5b. New printable conductive materials with certain amount of stretchability and good adhesion with the substrates, such as carbon nanotubes or silver nanowires, should be explored to further improve the

robustness of the devices, which could in turn lead to fully printed and stretchable devices in the near future.

3. Conclusion

In summary, we have demonstrated extremely flexible TFTs and integrated logic gates fabricated through a fully printed process using silver nanoparticles, $BaTiO_3$/PMMA composites, and semiconducting carbon nanotubes as the metals, insulators, and semiconductors, respectively. Owing to the ultrathin polyimide substrate as well as the superior mechanical flexibility of the gate dielectric and carbon nanotube network, the devices exhibit intriguing reliability even under extreme folding conditions. We also show that the device characteristics can be optimized individually by progressively increasing the amount of sSWCNTs printed into the channel region of the load resistor. To the best of our knowledge, this is one of the first reports on fully printed and foldable integrated logic gates using carbon nanotubes. The material platform and processing strategy presented here will be beneficial for the development of ubiquitous, low-cost, and large-area flexible electronic systems, such as organic light-emitting diode displays, electronic skins, wearable sensors, and actuators, on both plastic and elastomeric substrates using printing processes.

4. Experimental Section

Device Fabrication: An ultrathin polyimide (HD MicroSystems, PI-2525) film with a thickness of around 10 μm was spun coated (2000 rpm for 1 min) on a silicon handling wafer. Then, 20 nm SiO_2 was deposited on the PI substrate using electron beam deposition to facilitate the incubation of sSWCNTs. It should be pointed out that while the SiO_2 layer is used to significantly reduce the incubation time, it is not crucial and can be skipped to lower the fabrication cost. Similarly, uniform and dense sSWCNT networks can be obtained directly on polyimide by pretreating the surface with O_2 plasma and elongating the incubation time. Next, the surface was functionalized with poly-L-lysine aqueous solution (0.1% w/v, Sigma-Aldrich) for 5 min followed by deionized water (DI water) rinsing. The substrate was subsequently immersed in sSWCNT solutions (98% enrichment, NanoIntegris, Inc.) for 1 h to deposit uniform and high-density sSWCNT networks. This step was followed by DI water rinsing to remove the residual surfactants. Next, patterns of the S/D electrodes for the TFTs and interconnects for the logic gates were printed with Ag nanoparticle ink (PG-007AA from Paru Corporation, South Korea) using a GIX Microplotter (Sonoplot Inc.). Typical values for the finest feature size and overlap printing registration accuracy of our printing process are ≈30 μm and ≈±100 μm, respectively, which can be affected by many factors including the tip size, the viscosity and surface tension of the ink, and the wetting of the ink to the substrate surface. The printed Ag patterns were annealed at 180 °C for 10 min on a hotplate to evaporate the solvent and sinter the Ag nanoparticles. Next, hybrid dielectric inks comprised of $BaTiO_3$ nanoparticles and PMMA (PD-100 from Paru Corporation, South Korea) were printed (at a temperature of ≈60 °C) into the channel regions of the TFTs as the gate dielectric layer. The as-received ink contains $BaTiO_3$ nanoparticles and PMMA dispersed in diethylene glycol butyl ether. Before printing, the ink was diluted using the native solvent to facilitate the dispensing. The sSWCNTs out of the channel regions were then etched with O_2 plasma (60 W, 40 s) using the $BaTiO_3$/PMMA dielectric layer as a hard mask. After sSWCNT etching, another layer of $BaTiO_3$/PMMA was printed into the channel regions to repair the damage caused by O_2 plasma and to avoid potential gate leakage. Ag top-gate electrodes were subsequently printed and annealed to complete the fabrication of TFTs. Finally, multiple passes of sSWCNTs were printed into the channels of the load resistors, one layer at a time, until the optimal device characteristics were achieved. Once the fabrication was completed, the polyimide substrate was peeled off from the silicon handling substrate, resulting in an extremely flexible integrated circuit as shown in Figure 1b.

Device Characterization: Microscopic morphology of carbon nanotubes were recorded by a Hitachi S-4700II field-emission scanning electron microscope (FESEM). Transistor and circuit characteristics were measured using an Agilent B1500A semiconductor parameter analyzer. For bending tests, the data were collected while the device was rolled around cylinders with various diameters. Cyclic bending tests were performed by hand. For the folding tests, electrical measurements were conducted before and after the device was folded and squeezed using a tweezer for several times. All measurements were carried out under ambient conditions.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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